"Design Space Exploration of Full Adder Circuits: A Power-Delay-Area Perspective Across CMOS Technology Scaling"

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ABSTRACT:

As technology advances, digital circuits are becoming more complex, requiring efficient and power-conscious arithmetic units. This study explores the performance of full adders implemented with different CMOS technologies, focusing on power consumption, propagation delay, and area efficiency. Using simulation tools like Tanner EDA , we compare 45 nm and 90 nm technology nodes to understand the trade offs between speed, power, and area. Our findings indicate that hybrid full adders provide a better balance between power efficiency, performance, and area utilization, making them suitable for modern low-power applications.

Keywords: Full adder, CMOS technology, power efficiency, propagation delay, area optimization, VLSI.

I. INTRODUCTION

The evolution of modern digital electronics has been significantly influenced by advancements in Very Large Scale Integration (VLSI) technology. One of the core components in many digital systems, including arithmetic logic units (ALUs), digital signal processors (DSPs), and embedded control systems, is the full adder. As devices grow more compact and power-efficient, optimizing fundamental building blocks like full adders becomes essential. Full adders perform binary addition on three input bits (A, B, and Cin), producing a Sum and Carry output. The design of these adders in different technology nodes directly impacts the overall speed, power efficiency, and silicon area of digital systems.

This study focuses on comparing full adder designs using 90nm and 45nm CMOS technology nodes. With continuous downscaling of MOSFET dimensions, new challenges and benefits arise such as reduced parasitic and power consumption, but increased leakage and variability. By leveraging Electronic Design Automation (EDA) tools, particularly the Tanner EDA suite, this research explores how these scaling effects influence the performance of full adder circuits. The motivation behind this study is to identify which technology node delivers better efficiency in terms of power, delay, and chip area. This becomes increasingly relevant in the era of portable electronics and IoT, where devices must balance high computational capability with minimal energy usage. The research employs both pre-layout and post-layout simulations to provide a comprehensive understanding of circuit behavior in real-world scenarios. These findings are expected to guide future designs aiming for performance and efficiency at nanometer scales. This paper presents a comparative analysis of full adder designs implemented in 90nm and 45nm CMOS technologies. Using Tanner EDA tools including S-Edit for schematic design, T-Spice for simulation, and L-Edit for layout, we evaluate the performance of these circuits through extensive pre-layout and post-layout simulations. The parameters considered include average power dissipation, propagation delay, and chip area. Through this work, we aim to highlight the impact of technology scaling on full adder design and identify the most efficient approach for next-generation digital systems.

II. EXISTING METHOD

Conventional full adder designs utilizing 90nm CMOS technology predominantly rely on static CMOS logic for gate implementation. These designs feature standard complementary logic structures for constructing basic gates like XOR, AND, and OR, which are then interconnected to derive the Sum and Carry outputs. Due to the robustness, high noise immunity, and full voltage swing characteristics of static CMOS, these circuits are widely adopted across multiple domains. The 90nm technology node signified a milestone in VLSI design, offering an optimal trade-off between performance, power, and fabrication cost. Nevertheless,

this node also faced emerging limitations due to physical and electrical scaling issues. The reduction in supply voltage is constrained by threshold voltage requirements, preventing proportional voltage scaling and thereby keeping dynamic and static power consumption relatively high. Moreover, phenomena such as subthreshold leakage, gate oxide tunneling, and increased junction leakage have become substantial sources of power loss in 90nm designs. The 90nm technology node signified a milestone in VLSI design, offering an optimal trade-off between performance, power, and fabrication cost. Nevertheless, this node also faced emerging limitations due to physical and electrical scaling issues. The reduction in supply voltage is constrained by threshold voltage requirements, preventing proportional voltage scaling and thereby keeping dynamic and static power consumption relatively high. Moreover, phenomena such as subthreshold leakage, gate oxide tunneling, and increased junction leakage have become substantial sources of power loss in 90nm designs. Despite these drawbacks, 90nm full adder circuits are still relevant in legacy systems and specific industrial applications that prioritize design reliability and maturity over cutting-edge performance. Their design process is well understood, fabrication techniques are mature, and yield rates are typically high due to the stability of the node. These characteristics make them suitable for educational platforms, initial prototypes, and applications where cost constraints dominate performance requirements. In conclusion, while 90nm CMOS full adder designs provide an acceptable balance for many traditional applications, they fall short in meeting the demands of modern, high-performance, low-power systems. Their limitations in power efficiency, speed, and area drive the need to explore advanced technology nodes for optimized digital arithmetic circuits. In conclusion, while 90nm CMOS full adder designs provide an acceptable balance for many traditional applications, they fall short in meeting the demands of modern, high-performance, low-power systems. Their limitations in power efficiency, speed, and area drive the need to explore advanced technology nodes for optimized digital arithmetic circuits. Their constraints in terms of power consumption, speed, and silicon area highlight the necessity of transitioning to advanced technology nodes to achieve optimized digital arithmetic circuit designs.

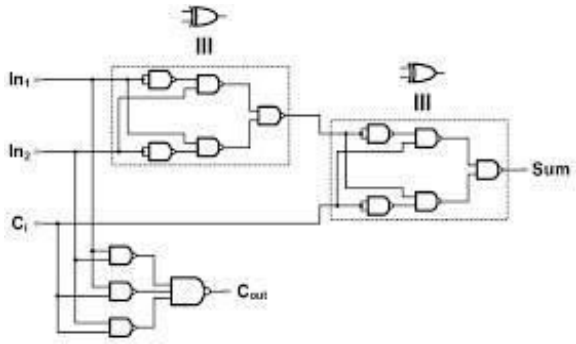


Fig:1 Full Adder Circuit

A Full Adder (FA) is a fundamental combinational circuit used for binary addition in digital systems. Unlike a Half Adder, which can only add two binary digits, a Full Adder incorporates a Carry-in (Cin) input, making it suitable for multi-bit addition. Full Adders play a crucial role in:

- Arithmetic Logic Units (ALUs)
- Digital Signal Processors (DSPs)
- Multipliers and Accumulators (MACs)

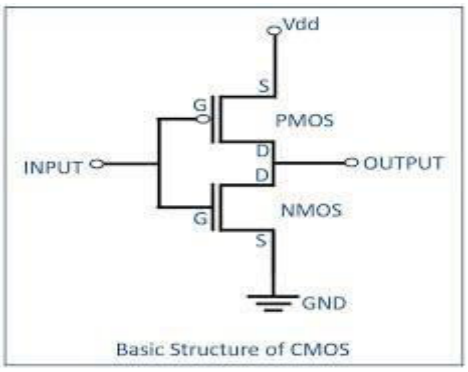


Fig:2 CMOS Inverter

Adders are widely used in:

• Arithmetic Circuits (Binary adders and multipliers)
• Digital Processors (ALUs in CPUs and GPUs)
• Error Detection and Correction (Parity checkers, checksum generators)
• Memory Address Calculation (RAM and cache memory structures)

CMOS Implementation of Full Adder

CMOS technology plays a critical role in designing low power, high-speed Full Adders. Several CMOS-based Full Adder designs include:

Conventional CMOS Full Adder (28 transistors): Uses complementary pull-up (PMOS) and pulldown (NMOS) networks but has high power consumption.

Transmission Gate Full Adder (TGA) (20-24 transistors): Reduces transistor count but experiences voltage degradation.

Mirror Adder (24 transistors): Offers a symmetrical layout for efficient high-speed applications.

XOR-XNOR Based Full Adder (12-16 transistors): Minimizes delays and power dissipation, making it ideal for low-power applications.

III. PROPOSED METHOD

The suggested system attempts to improve the performance of complete adders by utilising advanced CMOS technologies. To reduce power consumption and propagation delays, transistor sizing must be optimized, layout design refined, and new circuit topologies implemented. The suggested method includes comprehensive simulations utilising industry-standard tools such as Cadence

Virtuoso and Quartus II to assess various design configurations under a variety of operating situations.

Proposed Methodology:

The process includes the following important steps:

a. Design phase:

Multiple full adder designs have been developed using NAND and XOR gates in 45 nm and 90 nm manufacturing technologies.

b. Simulation: Utilize simulation software

To analyze timing waveforms, power consumption, and propagation delays manufacturing technologies.

c.Performance Evaluation: Compare the performance metrics of different designs based on power efficiency and speed.

d.Optimization: Refine designs based on simulation results to achieve optimal performance.

Conventional cmos full adder.

CMOS Technology Nodes:

Higher Nodes (90 nm, 180 nm):

Easier to fabricate and cost-effective for simple digital designs. These nodes exhibit lower leakage currents, making them suitable for low-frequency applications. However, they consume more power and occupy a larger chip area due to larger transistor sizes.

Medium Nodes (65 nm, 45 nm):

Offer a good balance between power efficiency, performance, and silicon area. These nodes support improved device density and switching speed compared to higher nodes.

***Advanced Nodes (22 nm, 14 nm, 7 nm*)**: Offer highspeed performance and reduced area usage but introduce manufacturing complexities. These nodes provide high-speed performance, significantly reduced power consumption, and minimized chip area—making them ideal for modern high-performance applications such as AI processors, smartphones, and high-end computing systems.

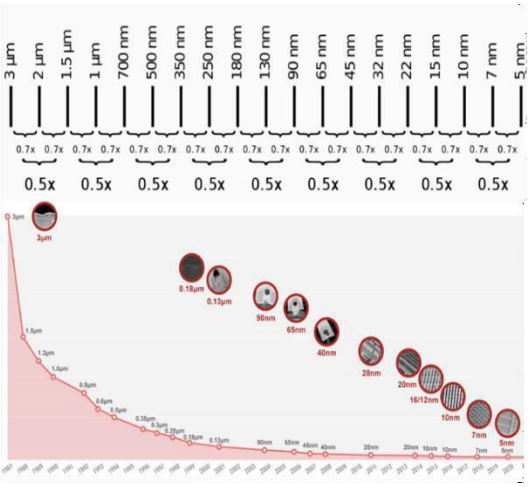


Fig:3 Technology nodes

Full Adder Designs:

The complete adder is a fundamental arithmetic circuit commonly used in digital systems. Its efficiency has a considerable impact on the overall performance of processors and arithmetic logic units. This study investigates the performance of various complete adder architectures implemented in various CMOS technologies, with a focus on metrics such as power dissipation, propagation latency, and transistor count. Several design strategies, including conventional, transmission gate, pass transistor logic, and hybrid techniques, have been investigated. The study evaluates their efficiency in terms of speed, power consumption, and space, providing information for optimising adder circuits for low-power and highspeed applications.

Traditional CMOS Full Adder: Uses 28 transistors, ensuring stable operation but consuming more power and chip area complementary pull-up and pull-down networks. However, it consumes more power and occupies a larger chip area, making it less suitable for low-power and area-constrained applications. The traditional CMOS full adder architecture utilizes 28 transistors, employing both PMOS and NMOS transistors in a complementary fashion to implement the logic functions. This design ensures robust and noise-immune operation, making it highly reliable for standard digital applications. However, due to the high transistor count, it results in increased power consumption and larger silicon area. As a result, it is less efficient for modern low-power, high-density VLSI systems where optimization of power and area is crucial.

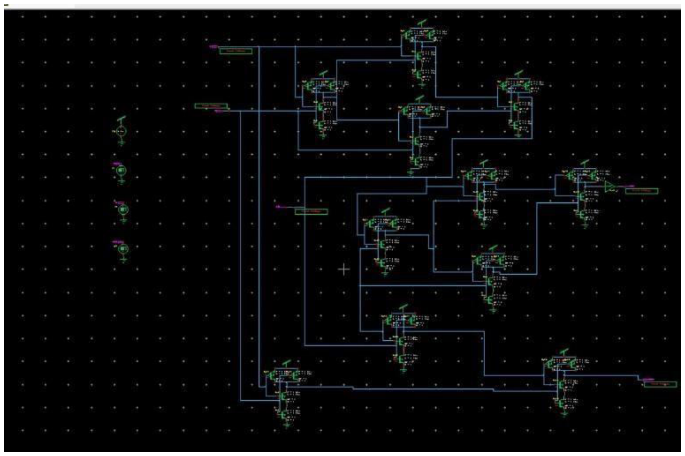


Fig:4 Full adder Circuit

Transmission Gate Logic(TGL) Full Adder:

Reduces transistor count and area but may suffer from voltage degradation.

***Hybrid Full Adder*:** Combines different logic styles (CMOS, pass transistor logic and transmission gates) to optimize performance and area utilization .

Power Consumption

***Dynamic Power*:** Dependent on switching activity and load capacitance.

***Leakage Power*:** Increases with scaling, requiring efficient reduction techniques.

Propagation Delay

Propagation delay directly affects the computational speed of digital circuits and is influenced by:

The number of transistor stages.

Resistance and capacitance of interconnects in deep sub micron nodes.

CMOS technologies boost performance, making them suited for current integrated circuits

Inputs			Outputs	
A	B	C_{in}	Sum	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Fig:5 Truth Table of Full Adder

Functionality and Truth Table
A Full Adder operates with three inputs:

- A – First operand bit
- B – Second operand bit
- Cin – Carry from the previous stage.

It generates two outputs:
Sum (S) – Result of binary addition
Carry-out (Cout) – Carry forwarded to the next stage.

Area Efficiency

Area efficiency is crucial in high-density VLSI designs and depends on:

Transistor Count: Fewer transistors reduce chip area and fabrication costs.

Layout Complexity: Optimized transistor placement minimizes area wastage.

***Technology Node*:** Smaller nodes improve area utilization but require careful design considerations.

Power-Delay Product (PDP) and Energy-Delay Product (EDP)

PDP: Measures the trade-off between power consumption and speed.

EDP: Evaluates energy efficiency, favoring low-power, high performance designs.

IV. RESULTS

The full adder designs were simulated in Tanner EDA using 45 nm and 90 nm CMOS nodes. The key parameters analysed were:

Power Consumption

•Dynamic Power: Dependent on switching activity and load capacitance.
•Leakage Power: Increases with scaling, requiring efficient reduction techniques.

Propagation Delay

Propagation delay directly affects the computational speed of digital circuits and is influenced by:
•The number of transistor stages.
•Resistance and capacitance of interconnects in deep submicron nodes.

Area Efficiency

Area efficiency is crucial in high-density VLSI designs and depends on:
•Transistor Count: Fewer transistors reduce chip area and fabrication costs
•Layout Complexity: Optimized transistor placement minimizes area wastage.
• Technology Node: Smaller nodes (e.g., 45 nm, 22 nm) enhance area utilization by allowing more components per unit area, but they demand precise design techniques to manage variability and leakage.

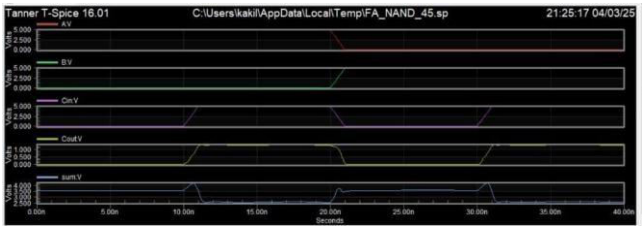


Fig:6 Timing waveform of full adder design with NAND gate using 45 nm technology.

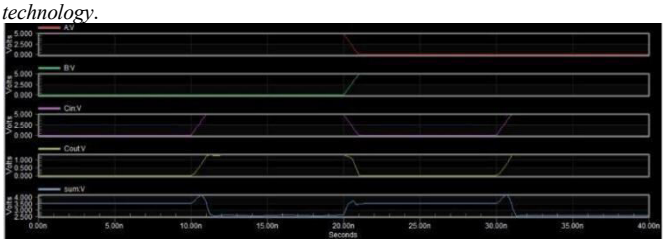


Fig:7 Timing waveform of full adder design with NAND gate using 90nm technology.

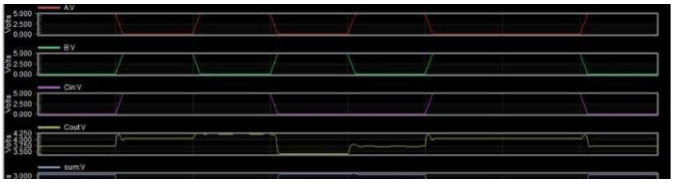


Fig:8 Timing waveform of full adder design with XOR and NAND gate using 45 nm technology.

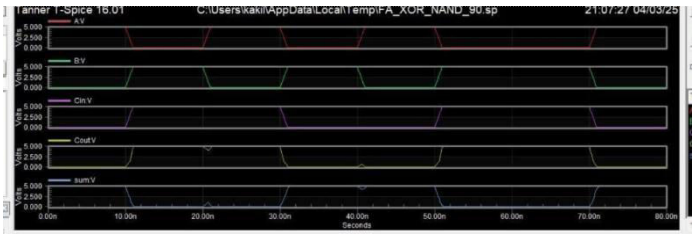


Fig:9 Timing waveform of full adder design with XOR and NAND gate using 90 nm technology

Our comparative analysis of 45 nm and 90 nm technology nodes revealed the following insights:

- **45 nm technology** demonstrates lower power consumption and improved area efficiency but suffers from higher leakage currents.
- **90 nm technology** has lower leakage and better noise margins but consumes more power and requires larger chip area.

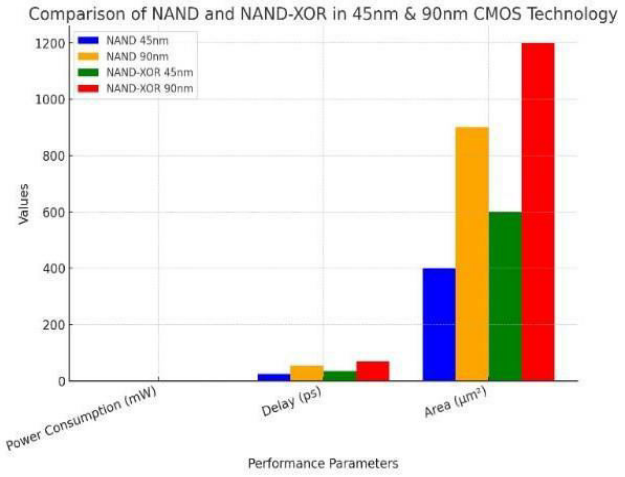
Table 1. Full Adder Using NAND GATE

Parameters	CMOS Technology	
	45 *nm*	**90 *nm***
Average Power (in µM)	3.43	5.73
Delay (in p sec)	0.72	0.87
Transistor Count	44	44

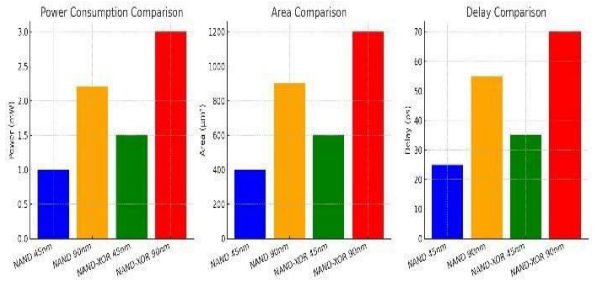
Table 2. Full Adder Using XOR and NAND GATE

Parameters	CMOS Technology	
	45 *nm*	**90 *nm***
Average Power (in µM)	2.09	3.79
Delay (in p sec)	0.96	1.37
Transistor Count	36	36

Graph:1Comparsion of NAND and NAND-XOR in 45nm&90nm CMOS Technology



Graph:2 Performance Comparison of Different CMOS Technologies



V. CONCLUSION

According to this study, 45nm CMOS technology performs significantly better than 90nm in terms of speed, area utilization, and power efficiency. NAND gate -based full adders at 45nm have the highest energy efficiency (PDP) of all the designs that were tested, which makes them perfect for low-power applications. On the other hand, complete adders based on NANDXOR gate offer a fair compromise between speed and power efficiency, which makes them ideal for high performance computing. To further improve efficiency, performance, and scalability in sophisticated digital circuits, future studies can investigate complete adders based on F in FET and GAAFET.

VI. REFERENCES

[1] R. Zimmermann and W. Fichtner, "Low power logic styles: CMOS versus pass transistor logic," IEEE Journal of Solid State Circuits, vol. 32, no. 7, pp. 1079- 1090,
1997. Available:
https://ieeexplore.ieee.org/document/596668

[2] A.U. Alam, N. Majid and S.K. Aditya,
"Layout Design of a 2-bit Binary Parallel Ripple Carry Adder Using CMOS NAND Gates with Microwind," *Dhaka Univ. J. Sci.*, 60(1): 103108, January 2012. Available: https://www.du.ac.bd

[3]Bhavani Prasad Y., Harish Babu N., Ramana Reddy K.V., Dhanabal R, "Comparative
Performance Analysis of XOR-XNOR Function Based High-Speed CMOS Full Adder Circuits," *International Conference on Reliability, Optimization and Information Technology*, India, pp. 432-436, February 2014. Available: https://www.icrit.org/xor-xnorcmos

[4]S. Sharma and R. Mehra, "Design,
Simulation and Comparative Analysis of CMOS Ripple Carry Adder," *IJRECE*, vol. 6, Issue 2, pp. 694-700, April-June 2018. Available: https://www.ijrece.org/ripplecarry

[5]Sheenu Rana and Rajesh Mehra, "Optimized CMOS Design of Full Adder using 45nm Technology," *International Journal of Computer Applications*, vol. 142, pp. 21-24, May 2016.
Available: https://www.ijcaonline.org/fulladder45n

[6]Amita, Mrs. Nitin Sachdeva, "Design and Analysis of Carry Look Ahead Adder Using
CMOS Technique," *IOSR Journal of Electronics and Communication Engineering (IOSR-JECE)*, vol. 9, Issue 2, pp. 92-95, March-April 2014. Available:
[7]https://www.iosrjournals.org/carrylookahead
M. Hemalatha et al., "Performance Analysis of a 1-Bit Full Adder Using 180 nm Technology," IJEE, vol. 3, no. 4, pp. 87-93, 2015. Available:
https://www.ijee.org/fulladder-180nm

[8]Bhavani Prasad Y. et al., "Comparative
Performance Analysis of XOR-XNOR Function Based CMOS Full Adder Circuits," ICRIT, pp. 432-436, 2014. Available:
https://www.icrit.org/xor-xnorcmos